* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to CMOS (Comlementary Metal Oxide Semiconductor) mold image sensors, and by dividing a light sensing portion and a circumference circuit, respectively, and forming them especially, it relates to the image sensors which reduced the layout man day sharply, and its manufacture method while improving the engine performance.
[0002]
[Description of the Prior Art] The conventional CMOS mold image sensors had the configuration equipped with the circumference circuit of only a lot to the light sensing portion formed by unifying. Drawing 9 is drawing showing the configuration of the conventional CMOS mold image sensors. On a substrate plane, the pixel array 10 arranges the pixel of the unit containing a photodiode in the shape of a matrix, and constitutes them. [two or more] According to the address signal from the outside, by the address decoder 11, the start address of the direction of a low (line) and the direction of a column (train) is generated, and low-scan shift register 12 and the column-scan shift register 13 are supplied. And according to a clock, with low - scan shift register 12, the row address which carries out a sequential shift is generated, and the word line corresponding to a row address in the pixel array 10 is driven by the low driver 14 from a vertical start address. On the other hand, according to a clock, from a horizontal start address, the column address which carries out a sequential shift is generated, and the bit line corresponding to a column address in the pixel array 10 is driven with the column-scan shift register 13. To the photo-electric-conversion output generated in the photodiode by this in the pixel specified by the row address and column address in the pixel array 10, by the noise-control circuit 15, a necessary noise control is performed and an output is generated. The clock control circuit 16 supplies a necessary clock to an address decoder 11, low-scan shift register 12, and the column-scan shift register 13 according to the clock signal from the outside.
[0003] Thus, through the noise-control circuit, one by one, the photo-electric-conversion output which generated a pixel array and its circumference circuit with the photodiode with which only a lot has and was specified according to the selected row address and selected column address of arbitration and which consists of an analog signal consisted of conventional image sensors so that it might be outputted outside.
[0004]
[Problem(s) to be Solved by the Invention] By the way, that the pixel array which takes charge of a photo-electric-conversion function in image sensors increases the number of pixels for the improvement in image quality has large-scale-ized gradually the semiconductor chip which is demanded, therefore carries a pixel array with the increment in the number of pixels. However, a chip scale follows on becoming large, and the effect of the wiring load of the pixel array on a substrate becomes large, therefore the working speed as image sensors falls, and there is a problem of having to stop having to lower a FUMU rate as a result. Moreover, in the case of a large-scale chip, there is a problem that the man day for the layout of a circuit design and the mask for substrate exposure increases remarkably.

[0005] This invention aims at offering the CMOS mold image sensors which can make the wiring load on a substrate small while it is made in view of an above-mentioned situation and can reduce the man day for a circuit design and mask layout.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, invention according to claim 1 While starting image sensors, connecting [dimensions / two] a pixel block which arranged two or more pixels in a line writing direction and the direction of a train in the direction of up Noriyuki, or the two directions of a train, arranging and forming a pixel array A low selection means to choose a read-out line of two or more pixels which form this pixel block in the direction of a train is arranged along an outside by the side of a train of each pixel block. While arranging a column selection means to choose as a line writing direction an output train of two or more pixels which form this pixel block, along an outside by the side of a line of each pixel block It is characterized by having arranged adjacently a noise-control means to perform a noise control of a pixel output for this every output train, for every above-mentioned column selection means.
[0007] While invention according to claim 2 relating to image sensors, and connecting [dimensions / two] a pixel block which arranged two or more pixels in a line writing direction and the direction of a train in the direction of up Noriyuki, and every two directions of a train, arranging and forming a pixel array A low selection means to choose a read-out line of two or more pixels which form this pixel block in the direction of a train is arranged along an outside by the side of a train of each pixel block. While arranging a column selection means to choose as a line writing direction an output train of two or more pixels which form this pixel block, along an outside by the side of a line of each pixel block It is characterized by having arranged adjacently a noise-control means to perform a noise control of a pixel output for this every output train, for every above-mentioned column selection means.
[0008] Invention according to claim 3 is characterized by constituting so that gain dispersion of an output amplifier of this both noise-controls means may be detected by measuring an output of a noise-control means of both pixel block based on [prepare a pixel for a sensitivity comparison / proofreading for every two pixel blocks, and] this pixel for a sensitivity comparison / proofreading image sensors according to claim 1 or 2 are started [noise control], and it connects [noise control / image sensors] in the direction of up Noriyuki, and/or the direction of a train.
[0009] Invention according to claim 4 relates to image sensors according to claim 3, and is characterized by constituting based on a detection result of the above-mentioned gain dispersion, so that gain dispersion of an output amplifier of both the above-mentioned noise-controls means may be amended.
[0010] Moreover, invention according to claim 5 relates to image sensors according to claim 1 or 2, and is characterized by establishing an analog-to-digital-conversion means to change into a digital signal an output which becomes the output side of each above-mentioned noise-control means from an analog signal from this noise-control means.
[0011] As opposed to a pattern of a pixel block which invention according to claim 6 required for image sensors, and arranged two or more pixels to two dimensions in a line writing direction and the direction of a train The 1st pattern which has arranged a pattern of a circumference circuit by the side of a train along an outside by the side of a train of this pixel block, and has arranged a pattern of a circumference circuit by the side of a line along an outside by the side of a line of this pixel block, The 2nd pattern which reversed this 1st pattern in a line writing direction or the direction of a train By exposing on a substrate using a mask for exposure arranged so that a pattern of each above-mentioned pixel block in these both patterns may be connected in a line writing direction or the direction of a train, may arrange and may form a pattern of a pixel array It is characterized by forming image sensors on this substrate.
[0012] As opposed to a pattern of a pixel block which invention according to claim 7 required for image sensors, and arranged two or more pixels to two dimensions in a line writing direction and the direction of a train The 1st pattern which has arranged a pattern of a circumference circuit by the side of a train along an outside by the side of a train of this pixel block, and has arranged a pattern of a circumference circuit by the side of a line along an outside by the side of a line of this pixel block, The 2nd pattern which reversed this 1st pattern to a line writing direction, and the 3rd pattern which reversed this 1st

pattern in the direction of a train, The 4th pattern which reversed this 1st pattern in a line writing direction and the direction of a train By exposing on a substrate using a mask for exposure arranged so that a pattern of each above-mentioned pixel block in this each pattern may be connected in a line writing direction and the direction of a train, may arrange and may form a pattern of a pixel array It is characterized by forming image sensors on this substrate.

[0013] As opposed to a pattern of a pixel block which invention according to claim 8 required for image sensors, and arranged two or more pixels to two dimensions in a line writing direction and the direction of a train A mask for exposure which has the 1st pattern which has arranged a pattern of a circumference circuit by the side of a train along an outside by the side of a train of this pixel block, has arranged a pattern of a circumference circuit by the side of a line along an outside by the side of a line of this pixel block, and was formed, A mask for exposure which has the 2nd pattern which reversed this 1st pattern in a line writing direction or the direction of a train is used. It is characterized by forming image sensors on this substrate by performing sequential exposure on one substrate so that a pattern of both the above-mentioned pixel block with this mask for both exposure may be connected in a line writing direction or the direction of a train, may arrange and may form a pattern of a pixel array.

[0014] As opposed to a pattern of a pixel block which invention according to claim 9 required for image sensors, and arranged two or more pixels to two dimensions in a line writing direction and the direction of a train A mask for exposure which has the 1st pattern which has arranged a pattern of a circumference circuit by the side of a train along an outside by the side of a train of this pixel block, and has arranged a pattern of a circumference circuit by the side of a line along an outside by the side of a line of this pixel block, A mask for exposure which has the 2nd pattern which reversed this 1st pattern to a line writing direction, A mask for exposure which has the 3rd pattern which reversed this 1st pattern in the direction of a train, A mask for ****** which has the 4th pattern which reversed this 1st pattern in a line writing direction and the direction of a train is used. It is characterized by forming image sensors on this substrate by performing sequential exposure on one substrate so that a pattern of each above-mentioned pixel block with this each mask for exposure may be connected in a line writing direction and the direction of a train, may arrange and may form a pattern of a pixel array.

[0015]

[Function] It is divided or quadrisected. the configuration of this invention -- the pixel array of one chip -- 2 -- by having the circumference circuit which forms a pixel block, respectively, resembles each pixel block, respectively, carries out reading appearance to the address generation section of a line writing direction and the direction of a train, and has a noise-control circuit to a signal Since division actuation and division read-out are performed independently, respectively, while being able to make small delay by the load of the wiring in a pixel array and being able to raise the frame rate of read-out, the man day of a circuit design and mask layout is sharply reducible.

[0016] Moreover, with another configuration of this invention, in an above-mentioned configuration, while gain dispersion of the output amplifier in the noise-control circuit of each pixel block is detectable by having prepared the pixel for a sensitivity comparison / proofreading for every two pixel blocks further, gain dispersion of each output amplifier can be readjusted based on a detection result.

[0017] Moreover, with still more nearly another configuration of this invention, since it was made to output after having the analog-to-digital converter for every pixel block and changing the output of each noise-control circuit into the digital signal, the noise based on taking about analog signal wiring for a long time mixed from gain dispersion, a power supply, the circumference circuit section of an output amplifier, etc. can be reduced.

[0018] By the method of this invention, a pixel array moreover, for every two division or quadrisected pixel block The pattern which formed by performing only the pixel block of a lot, the circuit design of only a circumference circuit, and mask layout layout when manufacturing the image sensors equipped with the circumference circuit, respectively, The pattern which reversed this pattern to the necessary sense is used. The pattern of each class Since it exposes on a substrate using the mask for exposure arranged and produced so that each pixel block may be connected and a pixel array may be formed, and image sensors are manufactured, the circuit design for creating the mask for exposure and the man day

of mask layout are reducible.
[0019] In the option of this invention, a pixel array moreover, for every two division or quadrisected pixel block The mask for exposure created with the pattern which formed by performing only the pixel block of a lot, the circuit design of only a circumference circuit, and mask layout layout when manufacturing the image sensors equipped with the circumference circuit, respectively, The mask for exposure created with the pattern which reversed the pattern of this mask for exposure to the necessary sense is used. Since it exposes by carrying out alignment so that each pixel block may be connected on a substrate and a pixel array may be formed, and image sensors are manufactured While the circuit design for creating the mask for exposure and the man day of mask layout are reducible Since the chip of one image sensors is created by performing 2 times or four exposure using two sheets or four masks for exposure, the image sensors of an a maximum of twice or 4 times as many area scale as this can be manufactured to the area which can be exposed with one mask for exposure.
[0020]
[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained with reference to a drawing. Explanation is concretely performed using an example.
<> 1st example drawing 1 is the block diagram showing the electric configuration of the image sensors which are the 1st example of this invention. As shown in drawing 1 , the outline configuration of the image sensors of this example is carried out from the pixel block 101,102, an address decoder 111,112, low-scan shift register 121,122, the column-scan shift register 131,132, the low driver 141,142, the noise-control circuit 151,152, and the clock control circuit 161,162.
[0021] Although it is arranged at the time of the mask layout of a substrate, or substrate exposure so that the pixel block 101,102 consists of a circuit block which divided the pixel array of one chip into two, and the pixel array 100 may be formed, when it arranges in succession on 1 plane to right and left (it omits a line writing direction and the following) or the upper and lower sides (it omits the direction of a train, and the following), these can carry out division actuation and division read-out independently by right and left or the upper and lower sides, respectively. According to the address signal from the outside, an address decoder 111,112 generates the start address of a perpendicular direction (it omits the direction of a train, and the following), and a horizontal direction (it omits a line writing direction and the following), and supplies it to low-scan shift register 121,122 and the column-scan shift register 131,132, respectively. Low - scan shift register 121,122 generates the row address which carries out a sequential shift from a vertical start address according to a clock, respectively. The low driver 141,142 drives the word line corresponding to a row address in the pixel block 101,102 according to the row address from low-scan shift register 121,122, respectively. According to a clock, from a horizontal start address, the column-scan shift register 131,132 generates the column address which carries out a sequential shift, and drives the bit line corresponding to a column address in the pixel block 101,102, respectively. To the photo-electric-conversion output from each pixel in the pixel block 101,102 by which reading appearance is carried out from each bit line, the noise-control circuit 151,152 performs a necessary noise control, and generates an output, respectively. The clock control circuit 161,162 supplies a necessary clock to address decoders 111 and 112, low-scan shift registers 121 and 122, and the column-scan shift register 131,132 according to the clock signal from the outside, respectively.
[0022] Next, actuation of the image sensors of this example is explained with reference to drawing 1 . In the pixel block 101,102, respectively by the clock control circuit 161,162 By supplying a clock to address decoders 111 and 112, low-scan shift registers 121 and 122, and the column-scan shift register 131,132 According to the perpendicular direction and the horizontal start address in the pixel block 101,102 generated by the address decoder 111,112, it sets to low - scan shift register 121,122. According to a clock, the address which carries out a sequential shift from a vertical start address is generated, respectively. Through the low driver 141,142, drive the word line corresponding to a row address in the pixel array block 101,102, and it sets to the column-scan shift register 131,132. According to a clock, from a horizontal start address, the column address which carries out a sequential shift is generated, and the bit line corresponding to a column address in the pixel block 101,102 is driven, respectively. And to the photo-electric-conversion output by which reading appearance is carried out through a bit line, by

the noise-control circuit 151,152, a necessary noise control is performed and an output is generated, respectively from the pixel specified by the row address and column address in the pixel block 101,102.
[0023] In the external circuit which is not illustrated, it has the memory for one frame (i.e., one chip) of a pixel array, for example. The image information based on the pixel block 101,102 outputted from the noise-control circuit 151,152, respectively is accumulated. By address actuation While the scan of a corresponding word line in the pixel block 101,102 is performed perpendicularly one by one continuously horizontally Necessary synthetic processing is performed and a video output is generated so that read-out of a bit line may be performed continuously one by one horizontally and the same output as read-out from the pixel array of one chip may be obtained.
[0024] Thus, in the image sensors of this example, since division read-out is performed while delay by the load of the wiring in a pixel array becomes small, since 2 ****s of read-out are carried out by the column side (or low side), the frame rate of read-out can be raised, therefore the engine performance of image sensors can be raised. Only one half of the circuit designs and mask layout of a portion of arbitration in the pixel array of one chip are performed. Furthermore, the remaining portion For example, so that the pattern reversed right and left (or upper and lower sides) may be prepared and both pixel block may be continuously located in a line with right and left (or upper and lower sides) at the time of mask layout or substrate exposure Since a pixel array is formed by arranging the circuit block divided into two, the layout man day of image sensors is sharply reducible.
[0025] <> 2nd example drawing 2 is the block diagram showing the electric configuration of the image sensors which are the 2nd example of this invention. As shown in drawing 2 , the outline configuration of the image sensors of this example is carried out from the pixel block 101,102,103,104, an address decoder 111,112,113,114, low-scan shift register 121,122,123,124, the column-scan shift register 131,132,133,134, the low driver 141,142,143,144, the noise-control circuit 151,152,153,154, and the clock control circuit 161,162,163,164.
[0026] Although it is arranged at the time of the mask layout of a substrate, or substrate exposure so that the pixel block 101,102,103,104 consists of a circuit block which quadrisected the pixel array of one chip, and pixel array 100A may be formed on 1 plane, when it arranges continuously up and down, right and left, these can perform division actuation and division read-out independently by right and left and the upper and lower sides, respectively. According to the address signal from the outside, an address decoder 111,112,113,114 generates a perpendicular direction and a horizontal start address, and supplies them to low-scan shift register 121,122,123,124 and the column-scan shift register 131,132,133,134, respectively. Low - scan shift register 121,122,123,124 generates the row address which carries out a sequential shift from a vertical start address according to a clock, respectively. The low driver 141,142,143,144 drives the word line corresponding to a row address in the pixel block 101,102,103,104 according to the row address from low-scan shift register 121,122,123,124, respectively. According to a clock, from a horizontal start address, the column-scan shift register 131,132,133,134 generates the column address which carries out a sequential shift, and drives the bit line corresponding to a column address in the pixel block 101,102,103,104, respectively. To the photo-electric-conversion output of each pixel in the pixel block 101,102,103,104 by which reading appearance was carried out from each bit line, the noise-control circuit 151,152,153,154 performs a necessary noise control, and generates an output, respectively. The clock control circuit 161,162,163,164 supplies a necessary clock to address decoders 111, 112, 113, and 114, low-scan shift registers 121, 122, 123, and 124, and the column-scan shift register 131,132,133,134 according to the clock signal from the outside, respectively.
[0027] Next, actuation of the image sensors of this example is explained with reference to drawing 2 . In the pixel block 101,102,103,104 Respectively by the clock control circuit 161,162,163,164 By supplying a clock to address decoders 111, 112, 113, and 114, low-scan shift registers 121, 122, 123, and 124, and the column-scan shift register 131,132,133,134 It can set to the pixel block 101,102,103,104 generated by the address decoder 111,112,113,114. According to a perpendicular direction and a horizontal start address, it sets to low-scan shift register 121,122,123,124. According to a clock, the row address which carries out a sequential shift from a vertical start address is generated, respectively. It can set to the pixel block 101,102,103,104 through the low driver 141,142,143,144.

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Drive the word line corresponding to a row address, and it sets to the column-scan shift register 131,132,133,134. According to a clock, from a horizontal start address, the column address which carries out a sequential shift is generated, and the bit line corresponding to a column address in the pixel block 101,102,103,104 is driven, respectively. And to the photo-electric-conversion output by which reading appearance was carried out through the bit line, by the noise-control circuit 151,152,153,154, a necessary noise control is performed and an output is generated, respectively from the pixel specified by the row address and column address in the pixel block 101,102,103,104.

[0028] In the external circuit which is not illustrated, it has the memory for one frame (i.e., one chip) of a pixel array, for example. The image information based on the pixel block 101,102,103,104 outputted from the noise-control circuit 151,152,153,154, respectively is accumulated. By address actuation While the scan of a corresponding word line in the pixel blocks 101,102 and 103,104 is performed perpendicularly one by one continuously horizontally Necessary synthetic processing is performed and a video output is generated so that the scan of a corresponding bit line in the pixel blocks 101,103 and 102,104 may continue perpendicularly, may be performed horizontally one by one and the same output as read-out from the pixel array of one chip may be obtained.

[0029] Thus, in the image sensors of this example, since division read-out is performed while delay by the load of the wiring in a pixel array becomes small, since 2 ****s of read-out are carried out by the column and low side, respectively, the frame rate of read-out can be raised, therefore the engine performance of image sensors can be raised. Only one fourth of the circuit designs and mask layout of a portion of arbitration in the pixel array of one chip are performed. Furthermore, the remaining portion For example, so that right and left and/or the pattern reversed up and down may be prepared and four pixel blocks may be continuously located in a line with right and left and the upper and lower sides at the time of mask layout or exposure of a substrate Since a pixel array is formed by arranging the quadrisected circuit block, the layout man day of image sensors is sharply reducible.

[0030] <> 3rd example drawing 3 is the block diagram showing the electric configuration of the image sensors which are the 3rd example of this invention. As shown in drawing 3 , the outline configuration of the image sensors of this example is carried out from the pixel block 101,102, an address decoder 111,112, low-scan shift register 121,122, the column-scan shift register 131,132, the low driver 141,142, the noise-control circuits 151A and 152A, the clock control circuit 161,162, and the pixel 171 for a sensitivity comparison / proofreading.

[0031] In this example, it has the same configuration as the pixel block 101,102, an address decoder 111,112, low-scan shift register 121,122, the column-scan shift register 131,132, the low driver 141,142, and the circuit element of the same sign in the 1st example indicated to be the clock control circuit 161,162 to drawing 1 , respectively, and since the same is said of those functions, below, the detailed explanation about these is omitted below, or it simplifies. The pixel 171 for a sensitivity comparison / proofreading is formed outside the effective pixel field of the pixel array 100, and reads the photo-electric-conversion output to the noise-control circuits 151A and 152A based on control of the control section which is not illustrated, respectively at the time of a test. While the noise-control circuits 151A and 152A perform a necessary noise control and generate an output to the photo-electric-conversion output from each pixel in the pixel block 101,102 by which reading appearance is carried out from each bit line, respectively While comparing the output level in the output amplifier of both the noise-controls circuits 151A and 152A based on the read-out output of the pixel 171 for a sensitivity comparison / proofreading and detecting gain dispersion based on control of the control section which is not illustrated It is constituted so that the gain of an output amplifier may be adjusted based on a detection result.

[0032] Next, actuation of the image sensors of this example is explained with reference to drawing 3 . In the pixel block 101,102, like the case of drawing 1 , division actuation and division read-out are performed, the photo-electric-conversion output from each pixel is generated according to assignment of a row address and a column address, a necessary noise control is performed, respectively and an output is generated in the noise-control circuits 151A and 152A. Under the present circumstances, according to control of the control section which is not illustrated, the existence and magnitude containing the output

amplifier in both the noise-controls circuits 151A and 152A of each gain dispersion can be known by comparing the output level of each output amplifier of the noise-control circuits 151A and 152A based on the output of the pixel 171 for a sensitivity comparison / proofreading. According to control of the control section which is not illustrated, based on the detection result of an output level furthermore, by controlling the gain of each output amplifier in both the noise-controls circuits 151A and 152A Gain of both the noise-controls circuits 151A and 152A can be made equal. By this As long as the capacity of each pixel which constitutes the pixel block 101,102 is equal, the output level from both the noise-controls circuits 151A and 152A at the time of an equal optical input level can become equal.

[0033] Thus, since the pixel array and the circumference circuit were divided two and have been arranged in the image sensors of this example While being able to make small delay by the load of the wiring in a pixel array, being able to raise the frame rate of read-out and being able to reduce the layout man day of image sensors sharply further While detecting gain dispersion of the amplifier for an output in each noise-control circuit corresponding to the pixel block divided and arranged by preparing the pixel for a sensitivity comparison / proofreading to the pixel block divided into two Gain dispersion of both output amplifiers can be amended.

[0034] <> 4th example drawing 4 is the block diagram showing the electric configuration of the image sensors which are the 4th example of this invention. As the image sensors of this example are shown in drawing 4 , the pixel block 101,102,103,104, An address decoder 111,112,113,114 and low-scan shift register 121,122,123,124, The column-scan shift register 131,132,133,134, The outline configuration is carried out from the low driver 141,142,143,144, the noise-control circuits 151A, 152A, 153A, and 154A, the clock control circuit 161,162,163,164, and the pixel 171,172,173,174 for a sensitivity comparison / proofreading.

[0035] In this example, it has the same configuration as the pixel block 101,102,103,104, an address decoder 111,112,113,114, low-scan shift register 121,122,123,124, the column-scan shift register 131,132,133,134, the low driver 141,142,143,144, and the circuit element of the same sign in the 2nd example indicated to be the clock control circuit 161,162,163,164 to drawing 2 , respectively, and the same is said of those functions. The pixel 171,172,173,174 for a sensitivity comparison / proofreading is formed outside the effective pixel field of the pixel array 100, and reads the photo-electric-conversion output to the noise-control circuit (151A, 152A) of a pair, (151A, 153A), (152A, 154A), and (153A, 154A) based on control of the control section which is not illustrated, respectively at the time of a test. The noise-control circuits 151A, 152A, 153A, and 154A While performing a necessary noise control and generating an output to the photo-electric-conversion output from each pixel in the pixel block 101,102,103,104 by which reading appearance is carried out from each bit line, respectively Based on control of the control section which is not illustrated, are based on the read-out output of the pixel 171,172,173,174 for a sensitivity comparison / proofreading. Respectively The noise-control circuit (151A, 152A) of a pair, (151A, 153A), While comparing the output level in the output amplifier of (153A, 154A), and (152A, 154A) and detecting gain dispersion between a pair each of output amplifiers, it is constituted so that the gain of both output amplifiers may be adjusted based on a detection result.

[0036] Next, actuation of the image sensors of this example is explained with reference to drawing 4 . In the pixel block 101,102,103,104, like the case of drawing 2 , division actuation and division read-out are performed, the photo-electric-conversion output from each pixel is generated according to assignment of a row address and a column address, a necessary noise control is performed, respectively and an output is generated in the noise-control circuits 151A, 152A, 153A, and 154A. Under the present circumstances, according to control of the control section which is not illustrated, are based on the read-out output of the pixel 171,172,173,174 for a sensitivity comparison / proofreading. By comparing the output level in the output amplifier of the noise-control circuit (151A, 152A) of a pair, (151A, 153A), (152A, 154A), and (153A, 154A), respectively The existence and magnitude containing the output amplifier in each noise-control circuits 151A, 152A, 153A, and 154A of each gain dispersion can be known. Based on control of the control section which is not illustrated, based on the detection result of an output level furthermore, by controlling the gain of each output amplifier in each noise-control circuits 151A, 152A, 153A, and 154A Gain of each noise-control circuits 151A, 152A, 153A, and 154A

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can be made equal. By this As long as the capacity of each pixel which constitutes the pixel block 101,102,103,104 is equal, the output level from each noise-control circuits 151A, 152A, 153A, and 154A at the time of an equal optical input level can become equal.
[0037] Thus, since the pixel array and the circumference circuit have been quadrisected and arranged in the image sensors of this example While delay by the load of the wiring in a pixel array can small-**, being able to raise the frame rate of read-out and being able to reduce the layout man day of image sensors sharply further By preparing the pixel for a sensitivity comparison / proofreading every two pixel blocks to the quadrisected pixel block While detecting gain dispersion of the amplifier for an output in each noise-control circuit corresponding to the pixel block divided and arranged, gain dispersion of both output amplifiers can be amended.
[0038] <> 5th example drawing 5 is the block diagram showing the electric configuration of the image sensors which are the 5th example of this invention. As shown in drawing 5 , the outline configuration of the image sensors of this example is carried out from the pixel block 101,102, an address decoder 111,112, low-scan shift register 121,122, the column-scan shift register 131,132, the low driver 141,142, the noise-control circuit 151,152, the clock control circuit 161,162, and the analog digital (A/D) converter 181,182.
[0039] In this example, it has the same configuration as the circuit element of the same sign in the 1st example indicated to be the pixel block 101,102, an address decoder 111,112, low-scan shift register 121,122, the column-scan shift register 131,132, the low driver 141,142, the noise-control circuit 151,152, and the clock control circuit 161,162 to drawing 1 , respectively, and the same is said of those functions. From the pixel block 101,102, reading appearance of A/D converter 181,182 is carried out for every column, and it changes and outputs the output which consists of an analog signal which had the noise control performed in the noise-control circuit 151,152 to a digital signal, respectively.
[0040] Next, actuation of the image sensors of this example is explained with reference to drawing 5 . In the pixel block 101,102, like the case of drawing 1 , division actuation and division read-out are performed, the photo-electric-conversion output from each pixel is generated according to assignment of a row address and a column address, a necessary noise control is performed, respectively and an output is generated in the noise-control circuit 151,152. A/D converter 181,182 changes and outputs the output which consists of an analog signal from the noise-control circuit 151,152, respectively to a digital signal.

[0041] In the visual equipment using image sensors, by taking about analog signal wiring for a long time, a possibility of being influenced of the noise mixed from gain dispersion, a power supply, a circumference circuit of an output amplifier, etc. may become high, and may cause dispersion in an image output level, and a noise. Then, an A/D converter is set near the pixel array, and a noise can be reduced, while leading about of an analog signal will decrease and a possibility of producing dispersion in an image output level will decrease, if the output which consists of an analog signal from a noise-control circuit is changed into a digital signal and it is made to output it.
[0042] Thus, in the image sensors of this example, since the A/D converter was formed in the noise-control circuit output and the image-sensors output was digital-signal-ized while the layout man day of image sensors was sharply reducible further by making small delay by the load of the wiring in a pixel array, and raising the frame rate of read-out, since the pixel array and the circumference circuit were divided two and had been arranged, level dispersion and the noise in a video output can be reduced.
[0043] <> 6th example drawing 6 is the block diagram showing the electric configuration of the image sensors which are the 6th example of this invention. As the image sensors of this example are shown in drawing 6 , the pixel block 101,102,103,104, An address decoder 111,112,113,114 and low-scan shift register 121,122,123,124, The column-scan shift register 131,132,133,134, The outline configuration is carried out from the low driver 141,142,143,144, the noise-control circuit 151,152,153,154, the clock control circuit 161,162,163,164, and the analog digital (A/D) converter 181,182,183,184.
[0044] In this example, it has the same configuration as the pixel block 101,102,103,104, an address decoder 111,112,113,114, low-scan shift register 121,122,123,124, the column-scan shift register 131,132,133,134, the low driver 141,142,143,144, and the circuit element of the same sign in the 2nd

example indicated to be the clock control circuit 161,162,163,164 to drawing 2 , respectively, and the same is said of those functions. From the pixel block 101,102,103,104, reading appearance of A/D converter 181,182,183,184 is carried out for every column, and it changes and outputs the output which consists of an analog signal which had the noise control performed in the noise-control circuit 151,152,153,154 to a digital signal, respectively.

[0045] Next, actuation of the image sensors of this example is explained with reference to drawing 6 . In the pixel block 101,102,103,104, like the case of drawing 2 , division actuation and division read-out are performed, a photo-electric-conversion output is generated from each pixel according to assignment of a row address and a column address, a necessary noise control is performed, respectively and an output is generated in the noise-control circuit 151,152,153,154. A/D converter 181,182,183,184 changes and outputs the output which consists of an analog signal from the noise-control circuit 151,152,153,154, respectively to a digital signal.

[0046] In the visual equipment using image sensors, by taking about analog signal wiring for a long time, a possibility of being influenced of the noise mixed from gain dispersion, a power supply, a circumference circuit of an output amplifier, etc. may become high, and may cause dispersion in an image output level, and a noise. Then, an A/D converter is set near the pixel array, and a noise can be reduced, while leading about of an analog signal will decrease and a possibility of producing dispersion in an image output level will decrease, if the output which consists of an analog signal from a noise-control circuit is changed into a digital signal and it is made to output it.

[0047] Thus, in the image sensors of this example, since the A/D converter was formed in the noise-control circuit output and the image-sensors output was digital-signal-ized while the layout man day of image sensors was sharply reducible further by making small delay by the load of the wiring in a pixel array, and raising the frame rate of read-out, since the pixel array and the circumference circuit had been quadrisected and arranged, level dispersion and the noise in a video output can be reduced.

[0048] <> 7th example drawing 7 is drawing explaining the manufacture method of the image sensors which are the 7th example of this invention. As opposed to the patterns 19A and 19B of the pixel block with which the mask 21 for exposure of this example arranged two or more pixels to two dimensions to the horizontal direction and the perpendicular direction as shown in drawing 7 (a) The pattern 20A1 of the circumference circuit by the side of a train which corresponds in the same subscript, and 20B1 The pattern which has arranged on the outside by the side of the train of the patterns 19A and 19B of a pixel block, respectively, and has arranged the pattern 20A2 of the circumference circuit by the side of a line and 20 B-2 on the outside by the side of the line of the patterns 19A and 19B of a pixel block, respectively is formed on one mask.

[0049] Pattern 19A of a pixel block here It is a thing corresponding to the pixel block 101 in the case of the 1st example. For example, the pattern 20A1 of a circumference circuit For example, it is a thing containing the pattern of the address decoder 111 in the case of the 1st example, low-scan shift register 111, the low driver 141, and the clock control circuit 161. The pattern of the circumference circuit 20A2 contains the pattern of the column-scan shift register 131 in the case of the 1st example, and the noise-control circuit 151. The same is said of the relation between pattern 19B of other pixel blocks, and the pattern 20B1 of a circumference circuit and 20 B-2. Moreover, it is also the same as when the configuration of a circumference circuit is a thing corresponding to the 3rd example and the 5th example.

[0050] The circuit design and mask layout in this case For example, after carrying out only to pattern 19A of a pixel block, the pattern 20A1 of a circumference circuit, and 20A2, By what reversed pattern 19A of a pixel block, the pattern 20A1 of a circumference circuit, and the pattern that consists of 20A2 right and left A mask 21 is created by forming pattern 19B of a pixel block, and the pattern 20B1 of a circumference circuit and 20 B-2, and arranging in the location where pattern 19B of a pixel block of this adjoins the right-hand side of pattern 19A of a pixel block.

[0051] thus, in manufacturing image sensors using the created mask 21 As shown in drawing 7 (b), by performing one exposure on a silicon substrate using a mask 21 The pixel array 220 the pixel blocks 22A and 22B come [pixel] to connect, Since exposure of the image-sensors substrate 24 with which a

circumference circuit (23A1, 23A2), and (23B1, 23 B-2) have been arranged, respectively is performed to the perimeter of each pixel blocks 22A and 22B Henceforth, the chip of image sensors can be manufactured by processing common knowledge, such as development.
[0052] Thus, by the manufacture method of the image sensors of this example, since the mask for exposure is created with one pixel block, the circuit design to that circumference circuit, the pattern formed of mask layout, and the pattern which reversed and formed this pattern in right and left and an image-sensors substrate is manufactured by one exposure with this mask for exposure, a man day required for the circuit design and mask layout of image sensors is reducible.
[0053] <> 8th example drawing 8 is drawing explaining the manufacture method of the image sensors which are the 8th example of this invention. As opposed to the patterns 19A, 19B, 19C, and 19D of the pixel block with which mask 21A for exposure of this example arranged two or more pixels to two dimensions to the horizontal direction and the perpendicular direction as shown in drawing 8 (a) The pattern 20A1 of the circumference circuit by the side of a train which corresponds in the same subscript, 20B1, and 20C 20D [1 and]1 It arranges on the outside by the side of the train of the patterns 19A, 19B, 19C, and 19D of a pixel block, respectively. The pattern which has arranged the pattern 20A2 of the circumference circuit by the side of a line, 20 B-2, and 20C 20D [2 and]2 on the outside by the side of the line of the patterns 19A, 19B, 19C, and 19D of a pixel block, respectively is formed on one mask.
[0054] Pattern 19A of a pixel block here It is a thing corresponding to the pixel block 101 in the case of the 2nd example. For example, the pattern 20A1 of a circumference circuit For example, it is a thing containing the pattern of the address decoder 111 in the case of the 2nd example, low-scan shift register 121, the low driver 141, and the clock control circuit 161. The pattern of the circumference circuit 20A2 contains the pattern of the column-scan shift register 131 in the case of the 2nd example, and the noise-control circuit 151. The same is said of the relation between the patterns 19B, 19C, and 19D of other pixel blocks, the pattern (20B1, 20 B-2) of a circumference circuit, (20C 20C [1 and]2), and (20D 20D [1 and]2). Moreover, it is also the same as when the configuration of a circumference circuit is a thing corresponding to the 4th example and the 6th example.
[0055] The circuit design and mask layout in this case For example, after carrying out only to pattern 19A of a pixel block, the pattern 20A1 of a circumference circuit, and 20A2, By what reversed pattern 19A of a pixel block, the pattern 20A1 of a circumference circuit, and the pattern that consists of 20A2 right and left Pattern 19B of a pixel block, and the pattern 20B1 of a circumference circuit and 20 B-2 are formed. This is arranged in the location where pattern 19B of a pixel block adjoins the right-hand side of pattern 19A of a pixel block. By what reversed pattern 19A of a pixel block, the pattern 20A1 of a circumference circuit, and the pattern that consists of 20A2 up and down Pattern 19C of a pixel block and pattern 20C 20C [1 and]2 of a circumference circuit are formed. ****** is arranged in the location where pattern 19C of a pixel block adjoins the pattern 19A bottom of a pixel block. Pattern 19A of a pixel block, the pattern 20A1 of a circumference circuit, and the pattern that consists of 20A2 by right and left and the thing which was reversed up and down Pattern 19D of a pixel block and pattern 20D 20D [1 and]2 of a circumference circuit are formed. Mask 21A for exposure is produced by arranging ****** in the location where pattern 19D of a pixel block adjoins pattern 19B [side / of pattern 19A of a pixel block / lower right] of a pixel block, and pattern 19C of a pixel block.
[0056] thus, in manufacturing image sensors using the created mask for exposure As shown in drawing 8 (b), by performing one exposure on a silicon substrate using mask 21A The pixel array 221 the pixel blocks 22A, 22B, 22C, and 22D come [pixel] to connect, Around each pixel blocks 22A, 22B, 22C, and 22D, respectively A circumference circuit (23A1, 23A2), Since exposure of image-sensors substrate 24A by which (23B1, 23 B-2), (23C 23C [1 and]2), and (23D 23D [1 and]2) have been arranged is performed, the chip of image sensors can be henceforth manufactured by processing common knowledge, such as development.
[0057] thus, by the manufacture method of the image sensors of this example One pixel block, the circuit design to the circumference circuit, and the pattern formed of mask layout, With the pattern which reversed and formed this pattern in right and left, the pattern which reversed up and down and was formed, and the pattern which reversed up and down with right and left, and was formed Since the

h g cg b eb cg e e

mask for exposure is created and an image-sensors substrate is manufactured by one exposure with this mask for exposure, a man day required for the circuit design and mask layout of image sensors is reducible.

[0058] Drawing 9 is drawing explaining the manufacture method of the image sensors which are the 9th example of this invention. Pattern 25A of a pixel block which arranged two or more pixels as show the mask for exposure of this example to drawing 9 (a) to two dimensions to the horizontal direction and the perpendicular direction, Mask 27A which has the pattern which consists of a pattern 26A1 of the circumference circuit by the side of a train, and a pattern 26A2 of the circumference circuit by the side of a line, It consists of mask 27B which has the pattern which consists of pattern 25B of a pixel block which arranged two or more pixels as shown in drawing 9 (b) to two dimensions to the horizontal direction and the perpendicular direction, and the pattern 26B1 of the circumference circuit by the side of a train and pattern 26 B-2 of the circumference circuit by the side of a line.

[0059] Pattern 25A of a pixel block here It is a thing corresponding to the pixel block 101 in the case of the 1st example. For example, the pattern 26A1 of a circumference circuit For example, it is a thing containing the pattern which consists of the address decoder 111 in the case of the 1st example, low-scan shift register 121, a low driver 141, and a clock control circuit 161. The pattern 26A2 of a circumference circuit contains the column-scan shift register 131 in the case of the 1st example, and the pattern which consists of a noise-control circuit 151. The same is said of the relation between pattern 25B of other pixel blocks, and the pattern 26B1 of a circumference circuit and 26 B-2. Moreover, it is also the same as when the configuration of a circumference circuit is a thing corresponding to the 3rd example and the 5th example.

[0060] It carries out only to pattern 25A of a pixel block, the pattern 26A1 of a circumference circuit, and 26A2, mask 27A is created, and the circuit design and mask layout in this case create mask 27B which has pattern 25B of a pixel block, the pattern 26B1 of a circumference circuit, and the pattern that consists of 26 B-2 by what reversed the pattern of mask 27A right and left.

[0061] thus, in manufacturing image sensors using the produced mask for exposure By using Masks 27A and 27B, and performing two exposure on a silicon substrate, performing alignment one by one, as shown in drawing 9 (c) While the pixel blocks 28A and 28B are connected [right and left] and form the pixel array 280 Since exposure of the image-sensors substrate 30 with which a circumference circuit (29A1, 29A2), and (29B1, 29 B-2) have been arranged, respectively is performed to the perimeter of each pixel blocks 28A and 28B Henceforth, the chip of image sensors can be manufactured by processing common knowledge, such as development.

[0062] thus, by the manufacture method of the image sensors of this example One pixel block, the circuit design only to the circumference circuit, and the mask for exposure created with the pattern formed according to mask layout, Since an image-sensors substrate is manufactured by performing two exposure one by one using the mask for exposure created with the pattern which reversed and formed this pattern in right and left, carrying out alignment A man day required for the circuit design and mask layout of image sensors is reducible. Moreover, by the manufacture method of the image sensors of this example, since two exposure is performed using two masks for exposure and the chip of one image sensors is created, the image sensors of an a maximum of twice as many area scale as this can be manufactured to the area which can be exposed with one mask for exposure.

[0063] Drawing 10 is drawing explaining the manufacture method of the image sensors which are the 10th example of this invention. Pattern 25A of a pixel block which arranged two or more pixels as show the mask for exposure of this example to drawing 10 (a) to two dimensions to the horizontal direction and the perpendicular direction, Mask 27A which has the pattern which consists of a pattern 26A1 of the circumference circuit by the side of a train, and a pattern 26A2 of the circumference circuit by the side of a line, Pattern 25B of a pixel block which arranged two or more pixels as shown in this drawing (b) to two dimensions to the horizontal direction and the perpendicular direction, Mask 27B which has the pattern which consists of a pattern 26B1 of the circumference circuit by the side of a train, and pattern 26 B-2 of the circumference circuit by the side of a line, Pattern 25C of a pixel block which arranged two or more pixels as shown in this drawing (c) to two dimensions to the horizontal direction and the

perpendicular direction, Mask 27C which has the pattern which consists of pattern 26C1 of the circumference circuit by the side of a train, and pattern 26C2 of the circumference circuit by the side of a line, It consists of mask 27D which has the pattern which consists of pattern 25D of a pixel block which arranged two or more pixels as shown in this drawing (d) to two dimensions to the horizontal direction and the perpendicular direction, and pattern 26D1 of the circumference circuit by the side of a train and pattern 26D2 of the circumference circuit by the side of a line.

[0064] Pattern 25A of a pixel block here It is a thing corresponding to the pixel block 101 in the case of the 2nd example. For example, the pattern 26A1 of a circumference circuit For example, it is a thing containing the pattern which consists of the address decoder 111 in the case of the 2nd example, low-scan shift register 121, a low driver 141, and a clock control circuit 161. The pattern 26A2 of a circumference circuit contains the column-scan shift register 131 in the case of the 2nd example, and the pattern which consists of a noise-control circuit 151. The same is said of the relation between the patterns 25B, 25C, and 25D of other pixel blocks, the pattern (26B1, 26 B-2) of a circumference circuit, (26C 26C [1 and]2), and (26D 26D [1 and]2). Moreover, it is also the same as when the configuration of a circumference circuit is a thing corresponding to the 4th example and the 6th example.

[0065] Perform the circuit design and mask layout in this case only to pattern 25A of a pixel block, the pattern 26A1 of a circumference circuit, and 26A2, and they create mask 27A. Mask 27B which has pattern 25B of a pixel block, the pattern 26B1 of a circumference circuit, and the pattern that consists of 26 B-2 by what reversed the pattern of mask 27A right and left is produced. Mask 27C which has the pattern which consists of pattern 25C of a pixel block by the thing and pattern 26C 1 and 26C of a circumference circuit2 which reversed the pattern of mask 27A up and down is created. Mask 27D which has the pattern which consists of pattern 25D of a pixel block by the thing and pattern 26D 1 and 26D of a circumference circuit2 which reversed the pattern of mask 27A up and down with right and left is created.

[0066] thus, in manufacturing image sensors using the created mask for exposure By using Masks 27A, 27B, 27C, and 27D, and performing four exposure on a silicon substrate, performing alignment one by one, as shown in this drawing (e) While the pixel blocks 28A, 28B, 27C, and 27D are connected [bottom / of the left upper right] and form the pixel array 281 Around each pixel blocks 28A, 28B, 27C, and 27D, respectively A circumference circuit (29A1, 29A2), Since exposure of image-sensors substrate 30A by which (29B1, 29 B-2), (29C 29C [1 and]2), and (29D 29D [1 and]2) have been arranged is performed, the chip of image sensors can be henceforth manufactured by processing common knowledge, such as development.

[0067] thus, by the manufacture method of the image sensors of this example One pixel block, the circuit design to the circumference circuit, and the mask for exposure created with the pattern formed according to mask layout, The mask for exposure created with the pattern which reversed and formed this pattern in right and left, By performing four exposure one by one using the mask for exposure created with the pattern which reversed up and down and was formed, and the mask for exposure created with the pattern which reversed up and down with right and left, and was formed, carrying out alignment Since an image-sensors substrate is manufactured, a man day required for the circuit design and mask layout of image sensors is reducible. Moreover, by the manufacture method of the image sensors of this example, since four exposure is performed using four masks for exposure and the chip of one image sensors is created, the image sensors of an a maximum of 4 times as many area scale as this can be manufactured to the area which can be exposed with one mask for exposure.

[0068] As mentioned above, although the example of this invention has been explained in full detail with the drawing, the concrete configuration was not restricted to this example, and even if there is modification of layout of the range which does not deviate from the summary of this invention etc., it is included in this invention. For example, it may be made to carry out the sequential operation of each pixel block and each circumference circuit to time of day which coincidence may be operated or is different, respectively. According to the latter method, the power for operating image sensors can be reduced. As a pixel for a sensitivity comparison / proofreading, the pixel within each pixel block is used, the output of a noise-control circuit based on this pixel is measured, and dispersion is detected, it may be

made to amend gain of both output amplifiers so that an output may become equal, and it becomes unnecessary moreover, to prepare the pixel for a sensitivity comparison / proofreading, and its control circuit outside an effective pixel field according to this method.

[0069]

[Effect of the Invention] according to [as explained above] the image sensors of this invention -- a pixel array and a circumference circuit -- 2 -- since it has divided, or quadrisected and arranged, delay by the load of the wiring in a pixel array can be made small, the frame rate of read-out can be raised, and the layout man day of image sensors can be reduced further sharply. Furthermore, gain dispersion can be amended while detecting gain dispersion of the amplifier for an output in each noise-control circuit corresponding to the pixel block divided and arranged in the pixel array since the pixel for a sensitivity comparison / proofreading was prepared to two division or the quadrisected pixel block. Moreover, a noise can be reduced, while leading about of an analog signal decreases and a possibility of producing level dispersion in a video output decreases, since the A/D converter was formed in the noise-control circuit output and the image-sensors output was digital-signal-ized. Moreover, since the chip of one image sensors is manufactured by performing 2 times or four exposure using two sheets or four masks for exposure, the image sensors of an a maximum of twice or 4 times as many area scale as this can be manufactured to the area which can be exposed with one mask for exposure.

[Translation done.]

PAT-NO: JP411150253A

DOCUMENT-IDENTIFIER: JP 11150253 A

TITLE: PHOTODETECTOR

PUBN-DATE: June 2, 1999

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APPL-NO: JP09318486

APPL-DATE: November 19, 1997

INT-CL (IPC): H01L027/14, G01B011/00 , H01L031/02 , H04N005/335

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a compact photodetector for constituting a light-tracking sensor without having an error caused by deviation in optical axis.

SOLUTION: A photodetector 10 is constituted mainly of a semiconductor substrate 12, where a quartered photodiode is formed at the center part of a device generating surface 12a and at the same time a photodiode array is formed around the periphery and a wiring board 18 for electrically connecting the semiconductor substrate 12 to the outside. In this case,

the semiconductor
substrate 12 is connected electrically and mechanically to
the wiring board 18
by a bump 20, so that the device generating surface 12a
faces opposite to the
wiring board 18. On the wiring board 18, a
signal-processing circuit is
constituted with a preamplifier and a signal selection
circuit.

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号

特開平11－150253

(43)公開日　平成11年(1999)６月２日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　27/14		Ｈ０１Ｌ　27/14	Ｄ
Ｇ０１Ｂ　11/00		Ｇ０１Ｂ　11/00	Ｅ
Ｈ０１Ｌ　31/02		Ｈ０４Ｎ　5/335	Ｚ
Ｈ０４Ｎ　5/335		Ｈ０１Ｌ　31/02	Ａ

審査請求　未請求　請求項の数７　ＯＬ　（全９頁）

(21)出願番号　特願平9－318486

(22)出願日　平成９年(1997)11月19日

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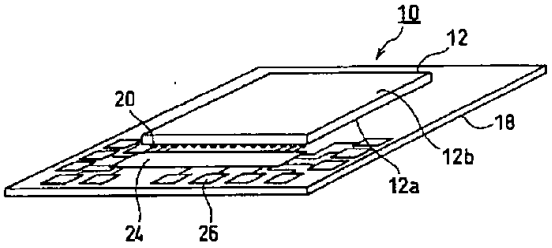
(54)【発明の名称】　光検出素子

(57)【要約】
【課題】　小型で、光軸ずれによる誤差のない光追尾センサを構成することができる光検出素子を提供する。
【解決手段】　光検出素子１０は、デバイス生成面１２ａの中央部に４分割フォトダイオード１４が形成されるとともにその周囲にフォトダイオードアレイ１６が形成されている半導体基板１２と、半導体基板１２と外部とを電気的に接続する配線基板１８とから主に構成され、半導体基板１２は、デバイス生成面１２ａが配線基板１８に対向するように、バンプ２０によって配線基板１８に電気的かつ機械的に接続されている。配線基板１８上には、プリアンプ及び信号選択回路を有する信号処理回路２４が構成されている。



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【特許請求の範囲】

【請求項1】　第1の主面の中央部に、4つのフォトダイオードを配列してなる4分割フォトダイオードが形成されていると共に、前記第1の主面上であって前記4分割フォトダイオードの周囲に、複数のフォトダイオードを配列してなるフォトダイオードアレイが形成されている半導体基板と、

前記半導体基板と外部とを電気的に接続する配線基板と、

を備え、

少なくとも前記4分割フォトダイオードを構成する各フォトダイオードは、それぞれバンプ接続によって前記配線基板に接続されている、ことを特徴とする光検出素子。

【請求項2】　前記フォトダイオードアレイを構成する各フォトダイオードは、それぞれバンプ接続によって前記配線基板に接続されている、ことを特徴とする請求項1に記載の光検出素子。

【請求項3】　前記配線基板は、

前記4分割フォトダイオードを構成する各フォトダイオードから出力された信号を増幅するプリアンプを有する信号処理回路を備えている、ことを特徴とする請求項1または2に記載の光検出素子。

【請求項4】　前記配線基板は、

前記4分割フォトダイオードを構成する各フォトダイオードから出力された信号を選択的に外部に取り出すための信号選択手段を有する信号処理回路を備えている、ことを特徴とする請求項1～3のいずれか1項に記載の光検出素子。

【請求項5】　前記配線基板は、

前記フォトダイオードアレイを構成する各フォトダイオードから出力された信号を増幅するプリアンプを有する信号処理回路を備えている、ことを特徴とする請求項1～4のいずれか1項に記載の光検出素子。

【請求項6】　前記配線基板は、

前記フォトダイオードアレイを構成する各フォトダイオードから出力された信号を選択的に外部に取り出すための信号選択手段を有する信号処理回路を備えている、ことを特徴とする請求項1～5のいずれか1項に記載の光検出素子。

【請求項7】　前記4分割フォトダイオードを構成する各フォトダイオードの受光面の大きさが、前記フォトダイオードアレイを構成する各フォトダイオードの受光面の大きさよりも大きい、ことを特徴とする請求項1～6のいずれか1項に記載の光検出素子。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、フォトダイオードを利用した光検出素子に関するものであり、特に測定対象から発せられる光（以下対象光という）を探索して追尾する、追尾センサとして利用されうる光検出素子に関するものである。

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【0002】

【従来の技術】近年、情報通信の大容量化、高速化のニーズに伴い、衛星間光通信の研究が盛んに行われている。中でも、1．55μm波長帯を利用した光通信は、地上における使用実績があり、地上と宇宙とで使用する光学部品を共通化できるというメリットがあるため、特に注目されている。

【0003】上記衛星間光通信のような移動体間通信を行う場合は、通信相手の位置を認識し、通信を行っている時間中は通信相手の位置を正確に追尾することが必要となる。そのため、通信相手の位置を探索して追尾する追尾センサは、通信相手の位置を探索するときは、空間的に広い範囲の対象光を検出する必要があり、通信相手の位置を探索した後に通信相手を追尾するときは、狭い範囲で正確且つ高速に対象光を検出する機能が要求される。

【0004】上記のような相反する要求の双方を満たすために、特開平6－214010号公報に記載されたような構成を有する追尾センサが広く用いられている。すなわち、応答速度は比較的遅いが広い視野角を有するCCDセンサから成る粗追尾センサと視野は狭いが高速応答が可能な4象限検出器とを備えた追尾センサである。このセンサは、通信相手から受光した光をミラーモジュールにより分割した後、これらの光をそれぞれの光軸上に配置されたCCDセンサ及び4象限検出器に導入し、通信相手位置の探索時はCCDセンサを用いて広範囲を探索し、通信相手位置を探索した後、通信相手を追尾するときは4象限検出器によって正確且つ高速に相手を追尾するという機能を有する。

【0005】上記のような追尾センサによって、広範囲から通信相手を探索し、探索後は通信相手を正確かつ高速に追尾することが可能となる。

【0006】

【発明が解決しようとする課題】しかし、追尾センサを上記に記載したように精追尾センサ及び粗追尾センサから構成し、受光した対象光を光学系によって双方のセンサに導入する光追尾センサには、以下に示すような問題点があった。

【0007】第1に、精追尾センサ、粗追尾センサを別々に備えるため、装置が大型化し、製造コストが増加してしまう。

【0008】第2に、受光した光を光学系によって分割して精追尾センサ、粗追尾センサに導入しているので、光学系の調整が困難であり、また精追尾センサと粗追尾センサとの光軸ずれが測定誤差の大きな要因になってしまう。

【0009】本発明は、上記問題点を解決し、小型で、製造コストを安く押さえられると共に、精追尾センサと

粗追尾センサとの光軸ずれによる誤差のない光追尾センサを構成することができる光検出素子を提供することを目的とする。

【0010】

【課題を解決するための手段】上記課題を解決するために、本発明の光検出素子は、第1の主面の中央部に、4つのフォトダイオードを配列してなる4分割フォトダイオードが形成されていると共に、第1の主面上であって4分割フォトダイオードの周囲に、複数のフォトダイオードを配列してなるフォトダイオードアレイが形成されている半導体基板と、半導体基板と外部とを電気的に接続する配線基板とを備え、少なくとも4分割フォトダイオードを構成する各フォトダイオードは、それぞれバンプ接続によって配線基板に接続されていることを特徴としている。

【0011】光検出素子を上記構成とすることにより、精追尾センサと粗追尾センサを同一素子上に形成することが可能となり、追尾センサの小型化が実現するとともに、精追尾センサと粗追尾センサとの光軸ずれが無くなる。また、4分割フォトダイオードを構成する各フォトダイオードが、それぞれバンプ接続によって配線基板に接続されていることにより、4分割フォトダイオードを構成する各フォトダイオードと配線基板とを電気的に接続するためのワイヤが不要となり、このワイヤによって4分割フォトダイオードまたはフォトダイオードアレイの受光面積が制限されることがなくなる。

【0012】本発明の光検出素子は、フォトダイオードアレイを構成する各フォトダイオードが、それぞれバンプ接続によって配線基板に接続されていることを特徴としてもよい。

【0013】上記構成にすることにより、フォトダイオードアレイを構成する各フォトダイオードと配線基板とを電気的に接続するためのワイヤが不要となり、このワイヤによって4分割フォトダイオードまたはフォトダイオードアレイの受光面積が制限されることがなくなる。

【0014】本発明の光検出素子は、配線基板が、4分割フォトダイオードを構成する各フォトダイオードから出力された信号を増幅するプリアンプを有する信号処理回路を備えていることを特徴としてもよい。

【0015】上記構成にすることによって、4分割フォトダイオードを構成する各フォトダイオードから出力された信号を増幅して外部に出力することができる。

【0016】本発明の光検出素子は、配線基板が、4分割フォトダイオードを構成する各フォトダイオードから出力された信号を選択的に外部に取り出すための信号選択手段を有する信号処理回路を備えていることを特徴としてもよい。

【0017】上記構成にすることにより、4分割フォトダイオードを構成する各フォトダイオードから出力された信号を選択的に外部に出力することができる。

【0018】本発明の光検出素子は、配線基板が、フォトダイオードアレイを構成する各フォトダイオードから出力された信号を増幅するプリアンプを有する信号処理回路を備えていることを特徴としてもよい。

【0019】上記構成にすることによって、フォトダイオードアレイを構成する各フォトダイオードから出力された信号を増幅して外部に出力することができる。

【0020】本発明の光検出素子は、前記配線基板が、フォトダイオードアレイを構成する各フォトダイオードから出力された信号を選択的に外部に取り出すための信号選択手段を有する信号処理回路を備えていることを特徴としてもよい。

【0021】上記構成にすることにより、フォトダイオードアレイを構成する各フォトダイオードから出力された信号を選択的に外部に出力することができる。

【0022】本発明の光検出素子は、4分割フォトダイオードを構成する各フォトダイオードの受光面の大きさが、フォトダイオードアレイを構成する各フォトダイオードの受光面の大きさよりも大きいことを特徴としてもよい。

【0023】上記構成にすることによって、ビームスポットが大きい対象光についても、4分割フォトダイオードによって適切な精追尾が実現できる。

【0024】

【発明の実施の形態】本発明の第1の実施形態に係る光検出素子を図面を用いて説明する。まず本実施形態に係る光検出素子の構成について説明する。図1は、本実施形態に係る光検出素子の斜視図、図2は本実施形態に係る光検出素子を構成する半導体基板をデバイス生成面から見た平面図、図3は本実施形態に係る光検出素子の平面図、図4は本実施形態に係る光検出素子を構成する半導体基板にバンプを形成した様子を模式的に表した図、図5は本発明の実施形態に係る光検出素子を構成する半導体基板と配線基板とを接続する様子を表した図、図6は本実施形態に係る光検出素子を構成する半導体基板と配線基板とを接続するバンプ接続部の拡大図である。

【0025】光検出素子10は、図1に示すように、デバイス生成面（第1の主面）12aに4分割フォトダイオード14及びフォトダイオードアレイ16が形成されている半導体基板12と、半導体基板12と外部とを電気的に接続する配線基板18とから主に構成され、半導体基板12はデバイス生成面12aが配線基板18に対向するように、バンプ20によって配線基板18に電気的かつ機械的に接続されている。

【0026】半導体基板12は、GaAsを基材としており、図2に示すように、そのデバイス生成面12aの中央部には、4つのフォトダイオードを配列してなる4分割フォトダイオード14が形成されている。また、4分割フォトダイオード14の周囲には、240（16×16－16）個のフォトダイオードを配列してなるフォ

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トダイオードアレイ１６が形成されている。ここで、フォトダイオードアレイ１６を構成する各フォトダイオードの受光面積（以下画素の大きさという）はそれぞれ等しくなっている。また、４分割フォトダイオード１４を構成する各フォトダイオードの画素の大きさはそれぞれ等しくなっており、かつ、フォトダイオードアレイ１６を構成する各フォトダイオードの画素の大きさの４倍の大きさとなっている。

【００２７】配線基板１８は、Ｓｉを基材としており、図３に示すような構成となっている。すなわち、配線基板１８上であって、半導体基板１２が固定される部分の下方には、半導体基板１２上に形成された４分割フォトダイオード１４及びフォトダイオードアレイ１６を配線基板１８に形成されたプリント配線２１と電気的に接続するためのボンディングパッド２２（図示せず）が形成され、電気的接続を容易ならしめている。また、配線基板１８上には、４分割フォトダイオード１４を構成する各フォトダイオードから出力された信号及びフォトダイオードアレイ１６を構成する各フォトダイオードから出力された信号をそれぞれ増幅するプリアンプと、４分割フォトダイオード１４を構成する各フォトダイオードから出力された信号を選択的に外部に取り出し、また、フォトダイオードアレイ１６を構成する各フォトダイオード１６から出力された信号を選択的に外部に取り出すための信号選択回路を有する信号処理回路２４が形成されている。この信号処理回路２４の入力端は、プリント配線２１を介してボンディングパッド２２と電気的に接続されている。さらに、配線基板１８上には引出電極パッド２６が形成されており、この引出電極パッド２６と信号処理回路２４の出力端とはプリント配線２１を介して電気的に接続されている。従って、引出電極パッド２６を介して、信号処理回路２４から出力された信号を外部から読み出すことが可能となる。

【００２８】半導体基板１２のデバイス生成面１２ａに形成された４分割フォトダイオード１４を構成する各フォトダイオード及びフォトダイオードアレイ１６を構成する各フォトダイオードは、バンプ接続によって配線基板１８上のボンディングパッド２２と接続されている。具体的には、図４に示すように、４分割フォトダイオード１４を構成する各フォトダイオード及びフォトダイオードアレイ１６を構成する各フォトダイオードのそれぞれにバンプ２０が形成された後、図５に示すように各バンプ２０のそれぞれが、配線基板１８上に設けられた、対応するボンディングパッド２２に接続される。従って、半導体基板１２のデバイス生成面１２ａと配線基板１８が対向する状態で電気的かつ機械的に固定される。その結果、本実施形態に係る光検出素子は、半導体基板１２の裏面１２ｂに入射した対象光を検出する裏面照射型光検出素子として作用することになる。

【００２９】図６はバンプ接続部の拡大図である。半導体基板１２のデバイス生成面１２ａには、４分割フォトダイオード１４を構成する各フォトダイオード及びフォトダイオードアレイ１６を構成する各フォトダイオードが形成されている位置に対応して、金またはアルミニウムなどからなるボンディングパット２３が設けられている。さらに、このボンディングパッド２３と配線基板１８上に設けられたボンディングパット２２とは、金または半田などからなるバンプ２０を介して電気的、かつ、機械的に接続されている。機械的接続強度を高めるために、半導体基板１２と配線基板１８との間隙に樹脂を流し込んで固定してもよい。

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【００３０】続いて、本実施形態に係る光検出素子の作用について説明する。本実施形態に係る光検出素子を光追尾センサとして用いる場合は、図７に示すように、光検出素子１０をパッケージ２００に組み込み、光検出素子１０から出力された信号に基づいて、光検出素子１０の受光面、すなわち半導体基板１２の裏面１２ｂを対象光の方向に動かす姿勢制御回路２０２を有する外部制御装置２０４を接続して用いることになる。パッケージ２００には対物レンズ２０１が固定されており、実際上無限遠からの平行光とみなされる対象光を、光検出素子１０に集光して入射させるようになっている。

【００３１】外部制御装置２０４の電源が投入されると、配線基板１８上に形成された信号処理回路２４内の信号選択回路によって、４分割フォトダイオード１４を構成する各フォトダイオード、及び、フォトダイオードアレイ１６を構成する各フォトダイオードを含む、全てのフォトダイオード（以下画素という）が順次選択され、一旦全ての画素から信号が読み出され、かつ、増幅される。ここで、信号の選択は、コンピュータなどで使用されているＲＡＭのデコーダ回路などと同様に、外部制御装置２０４内のＣＰＵ２０６によって指定された画素からの信号をランダムに選択することも可能となっている。

【００３２】読み出され、かつ、増幅された信号は、信号処理回路２４から外部制御装置２０４に伝送され、外部制御装置２０４に設けられたメモリ２０８内の、あらかじめ定められたアドレスにそれぞれ格納される。格納が終わると、外部制御装置２０４は入力待ちの状態となる。その後は、所定の時間間隔（例えば１ｍｓｅｃ）毎に、全ての画素から信号が読み出され、かつ、増幅され、その信号は上記メモリ２０８内に格納される。この状態では、全ての画素に入射する光信号を検出できるため、対象光を広範囲に検出できる。

【００３３】この状態において、いずれかの画素（複数でもよい）に光が入射すると、外部制御装置２０４は当該画素からの信号に基づいて入射位置を特定する。外部制御装置２０４内の姿勢制御回路２０２は、上記入射位置に基づき、当該対象光が光検出素子１２の中央部、すなわち４分割フォトダイオード１４の位置に入射するよ

うに、駆動装置２１０に駆動指示を送り、駆動装置２１０は、対象光に対するパッケージ２００の相対的な姿勢を調整する。この動作は、従来の粗追尾センサの機能に相当する。

【００３４】対象光が、光検出素子１２の中央部に形成された４分割フォトダイオード１４の位置に入射するように、パッケージ２００の姿勢が調整された後は、信号処理回路２４に形成された信号選択回路は、４分割フォトダイオード１４を構成する４つのフォトダイオードのみを選択し、これらの画素からの信号のみを読み出す。この状態では、外部制御装置２０４内の姿勢制御回路２０２は、対象光が４分割フォトダイオード１４の中心位置に入射するように、換言すれば、４分割フォトダイオード１４を構成する各フォトダイオードから信号が等しくなるように、逐次駆動装置２１０に指示を与え、駆動装置２１０が、パッケージの相対的な姿勢を調整することにより、対象光の入射方向の追尾を行う。この動作は、従来の精追尾センサの機能に相当する。この場合、信号を読み出す画素数が４つとなることから、読み出しの時間は、全ての画素から信号を読み出す場合と比較して、４／２５２＝１／６３となる。従って、極めて高速に信号を読み出すことができ、追尾対象を追尾するために十分な速度を得ることができる。

【００３５】続いて、本実施形態に係る光検出素子の効果について説明する。まず第１に、本実施形態に係る光検出素子１０は、精追尾センサとしての４分割フォトダイオード１４と粗追尾センサとしてのフォトダイオードアレイ１６とを同一の半導体基板１２上に形成しているため、精追尾センサと粗追尾センサを別体として構成する従来の光検出素子と比較して、光検出素子自体を小型化できるとともに、光検出素子を用いる追尾センサを小型化することが可能となる。

【００３６】第２に、本実施形態に係る光検出素子１０は、精追尾センサとしての４分割フォトダイオード１４と粗追尾センサとしてのフォトダイオードアレイ１６とを同一の半導体基板１２上に形成しているため、精追尾センサと粗追尾センサを別体として構成する従来の光検出素子と比較して、製造コストを小さく押さえることが可能となる。

【００３７】第３に、本実施形態に係る光検出素子１０は、精追尾センサとしての４分割フォトダイオード１４と粗追尾センサとしてのフォトダイオードアレイ１６とを同一の半導体基板１２上に形成しているため、精追尾センサと粗追尾センサを別体として構成し、受光した対象光を光学系によって双方のセンサに導入する従来の光検出素子と異なり、精追尾センサの光軸と粗追尾センサの光軸とを合わせる必要が無くなり、精追尾から粗追尾へ、または粗追尾から精追尾への切換が容易になる。

【００３８】第４に、本実施形態に係る光検出素子１０は、精追尾センサとしての４分割フォトダイオード１４と粗追尾センサとしてのフォトダイオードアレイ１６とを同一の半導体基板１２上に形成しているため、精追尾センサと粗追尾センサを別体として構成し、受光した対象光を光学系によって双方のセンサに分割して導入する従来の光検出素子と異なり、精追尾センサと粗追尾センサの双方に入射する対象光の強度を弱めることが無いため、精追尾センサと粗追尾センサとを同時に動作させることも可能となる。

【００３９】第５に、本実施形態に係る光検出素子１０は、半導体基板１２のデバイス生成面１２ａと配線基板１８とをバンプ接続によって接続し、裏面照射型光検出素子として作用させるため、ワイヤボンディングによる電気的接続を確保する必要が無くなる。従って、従来一体化を困難としていた、ワイヤによる開口面積の制限が除去され、一体化が実現するとともに、効率のよい光検出素子が構成できる。

【００４０】第６に、本実施形態に係る光検出素子１０は、半導体基板１２のデバイス生成面１２ａと配線基板１８とをバンプ接続によって接続し、裏面照射型光検出素子として作用させるため、ワイヤボンディングによる電気的接続を確保する必要が無くなる。従って、ワイヤの配置等に制限されることなく４分割フォトダイオード１４、各フォトダイオードアレイ１６及び光検出素子１０全体のサイズ等を自由に設計変更することが可能となる。

【００４１】第７に、本実施形態に係る光検出素子１０は、４分割フォトダイオード１４及びフォトダイオードアレイ１６を配線基板１８とを独立した半導体基板１２に形成し、この半導体基板１２を配線基板１８とをバンプ接続によって接続しているため、配線基板１８を形成する材料と異なる材料を用いて半導体基板１２を形成することが可能となる。従って配線基板１８を形成する材料としては安価な汎用材料を用いたとしても、半導体基板１２を形成する材料を適宜選択することにより、対象光の波長に合わせた適切な光検出素子を形成することが可能となる。

【００４２】本実施形態に係る光検出素子１０において、半導体基板１２のデバイス生成面１２ａに形成された４分割フォトダイオード１４の各画素は、フォトダイオードアレイ１６の各画素の大きさの４倍の大きさを有していたが、これは図８に示すように、フォトダイオードアレイ１６の各画素の大きさと同じであってもよい。ここで、４分割フォトダイオード１４の各画素の大きさは、対象光のスポットサイズを考慮して、対象光のスポットサイズよりも大きくすることが、精度向上のために好適である。

【００４３】また、本実施形態に係る光検出素子１０において、フォトダイオードアレイ１６は、中央部の４分割フォトダイオード１４が形成されている部分を除き、１６×１６の格子状に配列されていたが、これは必要な

精度、対象光の特徴などを考慮して、３２×３２、６４×６４などのN×N（Nは任意の整数）の格子状の配列としてもよい。また、１６×３２、１２８×５６などのN×M（N、Mはそれぞれ任意の整数）の格子状の配列とすることも可能である。

【００４４】さらに、本実施形態に係る光検出素子１０は、図９に示すように、配線基板１８上に４分割フォトダイオード１４用の引出電極パッド２８を設け、バンプ２０及びプリント配線２１を介して４分割フォトダイオード１４の各画素と電気的に接続した構成としてもよい。このような構成にすることで、４分割フォトダイオード１４の各画素からの信号を、フォトダイオードアレイ１６の各画素からの信号と独立して読み出すことが可能となり、精追尾センサと粗追尾センサを同時、かつ、極めて高速に動作させることができる。

【００４５】また、本実施形態に係る光検出素子１０は、半導体基板としてＧａＡｓを用いていたが、対象光の波長等を考慮して、Ｓｉ、Ｇｅ、ＩｎＳｂ、ＩｎＡｓ、ＩｎＧａＡｓ、ＧａＡｓ、ＨｇＣｄＴｅなどの他の材料を用いて形成することも可能である。

【００４６】また、本実施形態に係る光検出素子１０において、配線基板１８上に設けられた信号処理回路２４は、信号選択回路を有し、各画素からの信号をランダムに読み出すことが可能であったが、信号処理回路２４は、プリアンプは有するが信号選択回路は有しない構成になっていてもよい。この場合は、プリアンプによって増幅された各画素からの信号を、外部制御装置に取り込んでから、外部制御装置内で信号選択を行い、所望の画素のデータを得ればよい。

【００４７】次に、本発明の第２の実施形態に係る光検出素子を図面を用いて説明する。図１０は、本実施形態に係る光検出素子の斜視図、図１１は、本実施形態に係る光検出素子の平面図である。本実施形態に係る光検出素子４０が第１の実施形態に係る光検出素子１０と構成上異なる点は、配線基板４２上に、プリアンプ、信号選択回路等を備えた信号処理回路を持たないことである。

【００４８】従って、配線基板４２は図１１のようになる。すなわち、配線基板４２は信号処理回路を有さず、４分割フォトダイオード１４を構成するフォトダイオード及びフォトダイオードアレイ１６を構成するフォトダイオードの数と同数の引出電極パッド２６を有しており、各フォトダイオードは、バンプ２０及びプリント配線２１を介して上記引出電極パッド２６と電気的に接続されている。

【００４９】本実施形態に係る光検出素子４０を、第１の実施形態に係る光検出素子１０と同様の機能を持って使用するには、例えば、図１２（斜視図）及び図１３（平面図）に示すように、第１の実施形態に係る光検出素子１０の配線基板１８上に設けられた信号処理回路２４と同様の機能を有する外部信号処理基板１００を使用

すればよい。この構成にすれば、配線基板４２上に設けられた各引出電極パッド２６と信号処理基板１００上に設けられた各入力用パッド１０２とをワイヤ１０４を介して電気的に接続し、各画素からの信号を信号処理回路１０６によって増幅し、信号の選択を行なった後、出力用パッド１０８から外部制御装置に読み出されることになる。

【００５０】本実施形態に係る光検出素子４０も、第１の実施形態に係る光検出素子１０と同様の作用及び効果が期待できる。

【００５１】本実施形態に係る光検出素子４０において、配線基板４２上に形成された引出電極パッド２６は、図１１に示すように配線基板４２の１辺に沿って形成されていたが、これは、図１４に示すように、配線基板４２の４辺に分割して形成されていてもよい。このように形成することで、パッケージに格納するときの配線の自由度を増すことが可能となる。

【００５２】さらに、本実施形態の光検出素子４０は、図１５に示すように、配線基板４２上に４分割フォトダイオード用引出電極パッド２８を設け、バンプ２０及びプリント配線２１を介して４分割フォトダイオード１４の各画素と電気的に接続した構成としてもよいことは、第１の実施形態に係る光検出素子１０と同様である。

【００５３】また、本実施形態に係る光検出素子４０の配線基板４２は、信号処理回路を形成しないため、セラミック基板、ガラス基板などの絶縁性基板が任意に選択可能である。

【００５４】また、フォトダイオードアレイ１６の各画素の大きさに対する４分割フォトダイオード１４の各画素の大きさを自由に設定しうること、フォトダイオードアレイ１６の配列を自由に設定しうること、半導体基板としてＳｉなどの他の材料を用いることができることなどは、第１の実施形態に係る光検出素子１０と同様である。

【００５５】

【発明の効果】本発明の光検出素子は、中央部に４分割フォトダイオードを設け、その周囲にフォトダイオードアレイを設けた半導体基板と配線基板とをバンプ接続によって接続した構成となっている。半導体基板と配線基板とをバンプ接続によって接続することにより、従来一体化を困難としていた、ワイヤによる開口面積の制限が除去され、一体化が実現するとともに、効率のよい光検出素子が構成できる。

【００５６】また、精追尾センサとしての４分割フォトダイオードと粗追尾センサとしてのフォトダイオードアレイが同一基板上に形成されている本発明の光検出素子を用いることにより、光軸ずれによる誤差のない、安価でコンパクトな追尾センサの実現が可能となる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係る光検出素子の斜

視図である。

【図２】本発明の第１の実施形態に係る光検出素子の半導体基板をデバイス生成面から見た平面図である。

【図３】本発明の第１の実施形態に係る光検出素子の平面図である。

【図４】本実施形態に係る光検出素子を構成する半導体基板にバンプを形成した様子を模式的に表した図である。

【図５】本発明の実施形態に係る光検出素子を構成する半導体基板と配線基板とを接続する様子を表した図である。

【図６】バンプ接続部の拡大図である。

【図７】本実施形態に係る光検出素子を追尾センサとして用いる場合のシステム構成図である。

【図８】本発明の第１の実施形態に係る光検出素子に用いる半導体基板の変形例の平面図である。

【図９】本発明の第１の実施形態に係る光検出素子の変形例の平面図である。

【図１０】本発明の第２の実施形態に係る光検出素子の斜視図である。

【図１１】本発明の第２の実施形態に係る光検出素子の平面図である。

【図１２】本発明の第２の実施形態に係る光検出素子に、外部信号処理基板を接続した様子を表す斜視図である。

【図１３】本発明の第２の実施形態に係る光検出素子に、外部信号処理基板を接続した様子を表す平面図である。

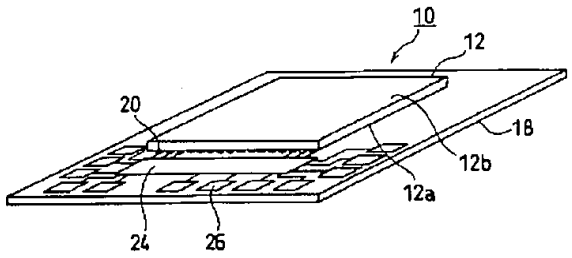
【図１４】本発明の第２の実施形態に係る光検出素子の変形例の平面図である。

【図１５】本発明の第２の実施形態に係る光検出素子の変形例の平面図である。

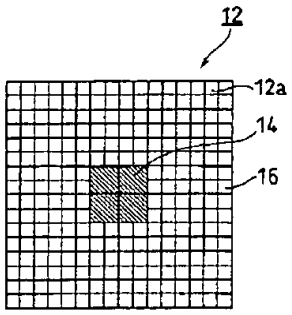
【符号の説明】

１０、４０…光検出素子、１２…半導体基板、１４…４分割フォトダイオード、１６…フォトダイオードアレイ、１８、４２…配線基板、２０…バンプ、２１…プリント配線、２２、２３…ボンディングパッド、２４…信号処理回路、２６、２８…引出電極パッド、１００…外部信号処理基板、１０２…入力用パッド、１０４…ワイヤ、１０６…信号処理回路、１０８…出力用パッド、２００…パッケージ、２０１…対物レンズ、２０２…姿勢制御回路、２０４…外部制御装置、２０６…ＣＰＵ、２０８…メモリ、２１０…駆動装置

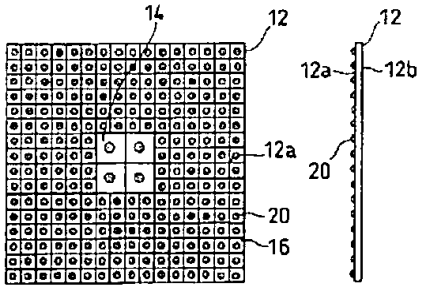
【図１】



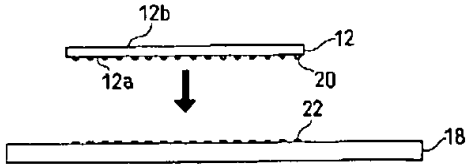
【図２】



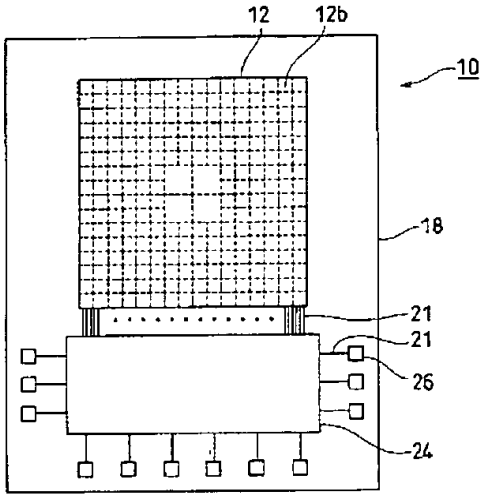
【図４】



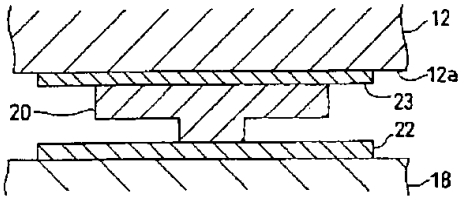
【図５】



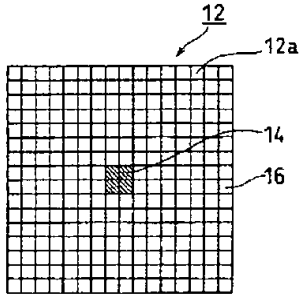
【図3】



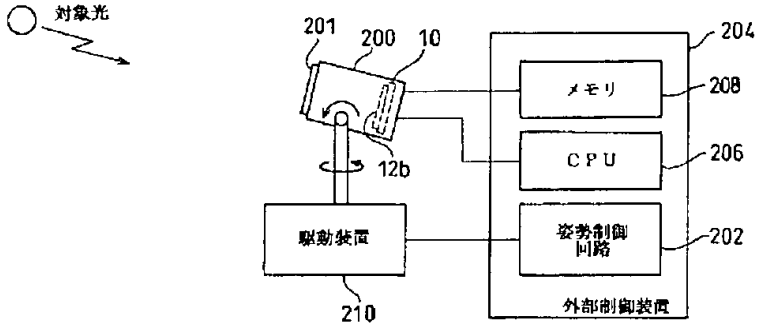
【図6】



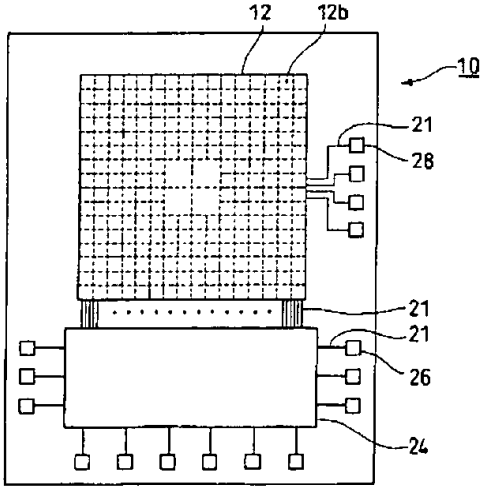
【図8】



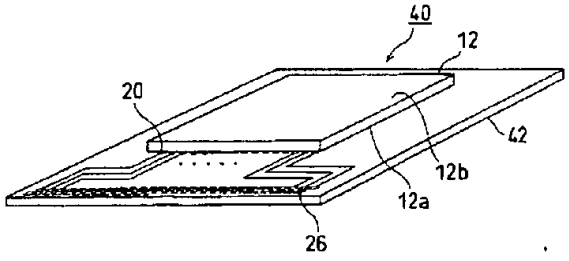
【図7】



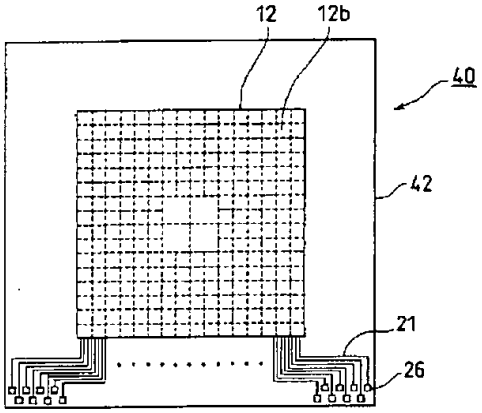
【図9】



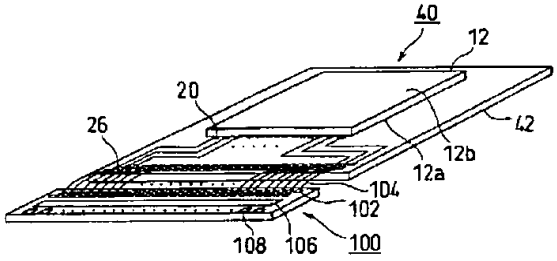
【図10】



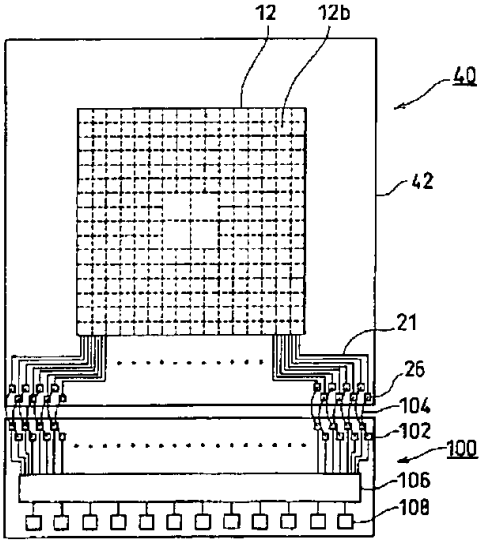
【図11】



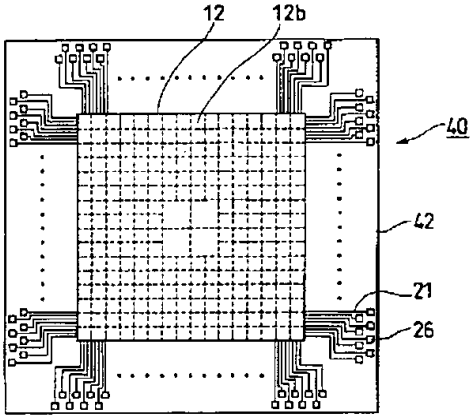
【図12】



【図13】



【図14】



【図15】